

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)

YOR920010104US (4370)

Application Number

Unassigned

Applicant(s)

Steven R. Fox, et al.

Filing Date

Herewith

Group Art Unit

Unassigned

U.S. PATENT DOCUMENTS

| *EXAMINER INITIAL | REF | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | FILING DATE IF APPROPRIATE |
|----------------------|-----|-----------------|----------|------------------|-------|----------|-------------------------------|
| RP | | 6,090,689 | 07/18/00 | Sadana, et al. | | | |
| LP | | 6,043,166 | 03/28/00 | Roitman, et al. | | | |
| RP | | 5,930,643 | 07/27/99 | Sadana, et al. | | | |
| | | 5,589,407 | 12/31/96 | Meyappan, et al. | | | |
| | | 5,519,336 | 05/21/96 | Liu, et al. | | | |
| | | 5,288,650 | 02/22/94 | Sadow | | | |
| | | 5,279,978 | 01/18/94 | See, et al. | | | |
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| | | 4,902,642 | 02/20/90 | Mao, et al. | | | |
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FOREIGN PATENT DOCUMENTS

| REF | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUBCLASS | Translation | |
|-----|-----------------|----------|---------|-------|----------|-------------|----|
| | | | | | | YES | NO |
| RP | JP 63 217657 | 09/09/88 | Japan | | | | |
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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| RP | | Wolf, S., "Silicon Processing for the VLSI ERA", Vol. 2: Process Integration, 1990, pp. 72-73 |
| 1 | | White, A.E., et al., "The role of implant temperature in the formation of thin buried oxide layers", BEAM-SOLID INTERACTIONS AND TRANSIENT PROCESSES SYMPOSIUM, BOSTON, MA, USA, 1-4 DEC. 1986, pp. 585-590, XP000922701 |

EXAMINER

Rm Pompey

DATE CONSIDERED

12-22-05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.